SOC MPEG-2 Video Decoder IP Core Datasheet

System-On-Chip (SOC) Technologies

Revision 6.0

1. Product Overview

The SOC MPEG-2 video decoder is a single core solution that supports single or multi-channel MPEG-2 video decoding for all industry standard resolutions including QVGA, SD and HD up to 60fps.

Key Features	
Profile & Level	High Profile and High Level
Chroma Format	4:2:0 or 4:2:2
Resolution	QVGA, SD, HD and custom
Frame Rate	Up to 60fps
Precision	8 bits
Input Stream	Transport or Elementary
Latency	0.25 - 4 frames

SOC can provide the MPEG-2 video decoder IP core for AMD (Xilinx) and Intel (Altera) FPGAs. SOC also offers an all-in-one decoder module based on the MPEG-2 video decoder IP core.

The SOC MPEG-2 video decoder is implemented based on SOC's proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has the significant advantages of high-speed (low latency) and small footprint (low power), while still providing high video quality and high resolution.

The SOC MPEG-2 IP core is a High Profile decoder with Simple and Main Profiles available, providing a subset of features in order to fit smaller FPGAs. It automatically detects and decodes 4:2:0 and 4:2:2 streams, and has 8-bit depth support, which makes it suitable for consumer products.

Users are able to control the operations of the decoder using the integrated user API. The API user manual is provided with the IP core and module.

The MPEG-2 decoder core can be customised into the following versions:

1. **Standard Version:**
   A balanced system optimised for key factors of logic resource utilisation and performance supporting I+P GOP structure.

2. **I-Frame Version:**
   The I-Frame version implements intra-prediction (I-Frames) only, without motion vector predictions. This reduces the logic resources and simplifies decoder complexity, allowing for very high channel density in a single FPGA.

3. **Other Versions:**
   Other special versions of the SOC MPEG-2 decoder, such as multi-channel and video scaling, are also available. Please contact SOC for product details.

The SOC decoder series can be integrated with an audio decoder to provide an all-in-one decoding solution. SOC can also integrate network modules, UDP-IP, Ethernet MACs into the design to produce full system-on-chip systems.

2. The SOC MPEG-2 Video Decoder Architecture

The SOC MPEG-2 video decoder is a self-contained FPGA IP core that can be either placed as a standalone core into a single FPGA or integrated with other logic blocks in the same FPGA for custom applications.

The block diagram of the IP core can be seen in Figure-1. All of the blocks in the design are implemented in hardware without embedded processors or embedded software, which offers high speed, low logic resource consumption, and low power.

Input to the decoder is a standard MPEG-2 elementary or transport stream. The output of the decoder is a video stream for standard display devices with frames properly ordered.

The decoder is capable of recovering decoding operations if the input stream contains errors and/or is corrupted during transmission. In the event that significant decoding errors occur, the last stable decoded frame will be displayed until the core receives a stable stream.

The SOC H.264 decoder requires one external clock source. The decoder also requires an external DDR3 or DDR4 memory with a minimum size depending on the resolution and the core's requirements. See section 6 "Targeted FPGAs and Logic Resources" for more information.

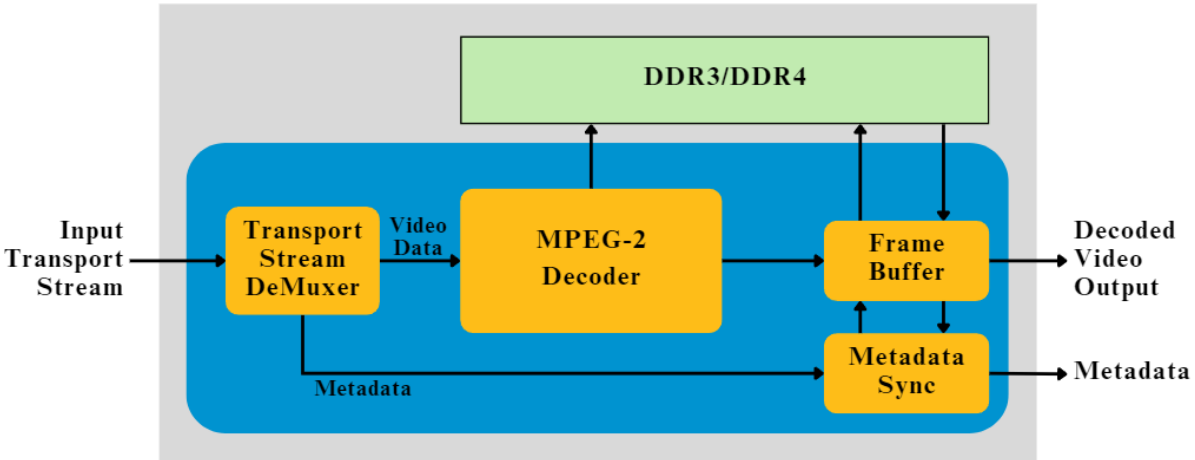

Figure-1 Block Diagram of SOC MPEG-2 Video Decoder

3. The MPEG-2 and Audio Decoder Solutions

SOC provides three MPEG-2 and audio decoder solutions:

1. **FPGA-DSP Solution:**
   For FPGAs that do not have an embedded ARM processor, an external DSP is used for audio decoding. Figure-2 shows the architecture of this system. The audio signal is sent to the external DSP (Blackfin BF512) for decoding. The decoded audio is sent back to a synchronisation module in the FPGA to ensure the video and audio are synchronised before outputting the data.

2. **Single FPGA Solution:**
   For FPGAs that have an embedded ARM processor, the ARM processor is used for audio decoding while the video decoder IP core uses the logic part of the FPGA. Figure-3 provides a block diagram for this single chip solution. The user must instantiate the HPS/PS for the system to work correctly. A guide for this will be provided with delivery of the IP core or module.

3. **PCM Pass Through Solution:**
   Audio data can be unpacked from the transport stream as PCM data which is then synchronised and output with the video.

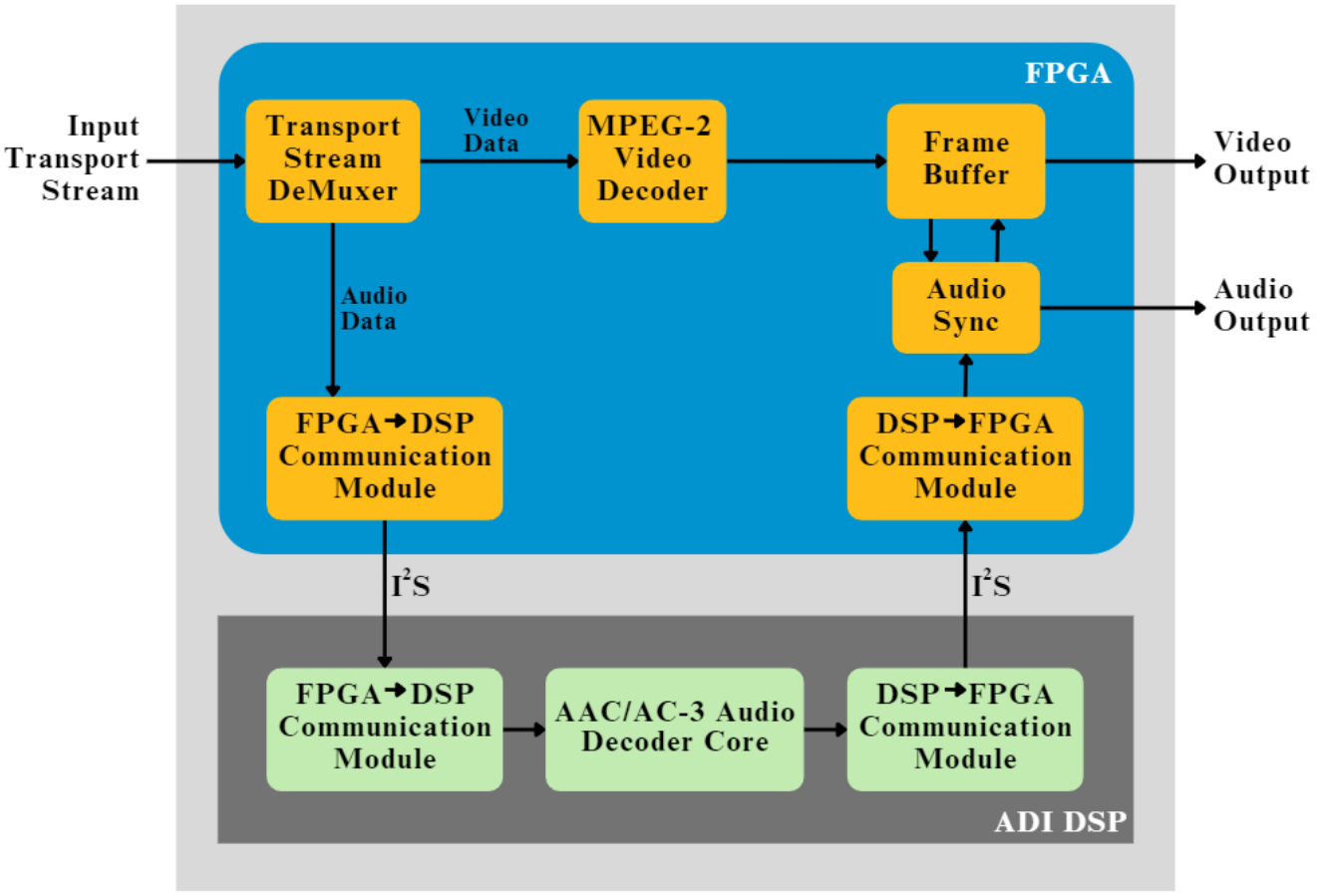

Figure-2 Block Diagram of the FPGA-DSP Video/Audio Decoder Solution

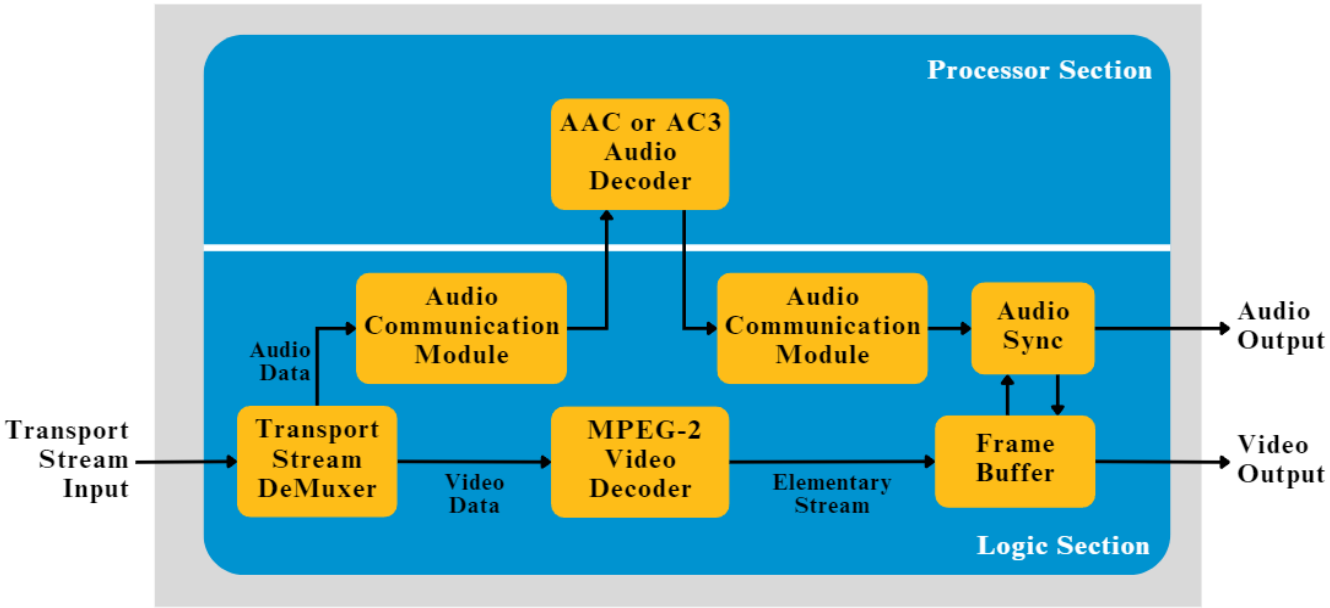

Figure-3 Block Diagram of the Single FPGA Video/Audio Decoder Solution

4. Video Technical Specifications

Conformance Standard:
MPEG-2/H.262 (ISO/IEC 13818-2)

Profiles:
- High Profile
- Main Profile
- Simple Profile

Chroma Format:
- 4:2:0
- 4:2:2

Precision:
- 8 bits

Resolution:
- 640x480 (QVGA)
- 1280x720 (SD)
- 1920x1080 (HD)
- Other resolutions available upon request

Frame Rate:
The SOC decoder supports all industry standard frame rates, including the following:
- 10fps
- 29.97fps
- 30fps
- 50fps
- 59.95fps
- 60fps
- Other frame rates available upon request

Supported Frame Types:
- I Frame
- P Frame
- B Frame

Latency:
The SOC MPEG-2 decoder has very low latency due to its hardware implementation. Table-1 shows an example of the different decoding engine latencies depending on performance requirements. Latency can vary based on different streams and their coding structures.

Latency	Supported GOP	Performance
< ¼ Frame	I, I+P	Standard
1 Frame	I, I+P	High
2-4 Frames	I, I+P, I+P+B	Very High

Table-1 The latency associated with each supported GOP and its associated performance

Bit Rate:
The decoder typically has an achievable bit rate of up to 60 Mbps but is dependent on the chosen fabric.

Power:
The power consumption that the IP core uses is based on many factors such as resolution, frame rate, number of channels, and core settings. Table-2 shows the power consumption for the different versions at a resolution of 1920x1080 and frame rate of 60 fps.[1]

Version	Power Consumption
Standard	1W
I-Frame	0.8W

Table-2 The power consumption associated with each version at 1920x1080 @60fps

[1] Power consumption estimates are for the decoder IP core only and do not include the vendor DDR controller or external memory.

5. Audio Technical Specifications

Conformance Standard:
HE-AAC (ISO/IEC 14496-3), MPEG-2 Layer-2

Audio Sample Rate:

- 44.1 kHz
- 48 kHz

Audio Bit Rate:
The total audio bit rate for stereo (left and right) audio decoding mode. Table-3 describes the different audio bit rates associated with each audio solution.

Audio Solution	Bit Rate (kbps)
FPGA-DSP	32-128
FPGA-ARM	16-384

Table-3 Audio bit rate for each audio solution

6. Target FPGAs and Logic Resources

The SOC MPEG-2 decoder IP core is available for both Xilinx and Altera FPGAs as long as they meet the logic resource and clock speed requirements.[2]
Logic resources are for the **CODEC only**. Additional resources are required depending on the final IP core design requirements (Transport Stream Support, Resolution requirement, Input video mode, DDR Configuration etc..).

DDR3/DDR4 Memory Minimum Based on Resolution

The decoder core requires a certain amount of DDR memory capacity and bandwidth in order to run. The requirements change depending on the highest resolution and core features the user desires. Table-4 describes the DDR requirements based on 1 channel 60fps and 8 bit pixel depth.[3]

DDR Memory Capacity	Bandwidth (Gbps)		
	I	I+P	I+P+B
128 MBytes	4.4	13.2	25.8

Table-4 The estimated DDR3/DDR4 memory requirements

Logic Resources on Xilinx FPGAs

The logic resources required on Xilinx FPGAs by the decoder IP core are listed in the following table. URAM can be used on available devices. Table-5 describes the resource usage for HD streams.

Resource Type	Version	
	Standard	I-Frame
LUTs	14K	11K
B-RAM	1Mb	0.6Mb
DSPs	54	54

Table-5 Logic resource utilisation of the HD decoder on a Xilinx FPGA

[2] Resource tables are subject to change and may vary depending on FPGA fabric.
[3] 10 bit requires 30% more bandwidth and double the capacity

Logic Resources on Altera FPGAs

The logic resources required on Altera FPGAs by the decoder IP core are listed in the following table. Table-6 describes the resource usage for HD streams.

Resource Type	Version	
	Standard	I-Frame
ALMs	8.8K	6.9K
B-RAM	1Mb	0.6Mb
DSPs	54	54

Table-6 Logic resource utilisation of the HD decoder on an Altera FPGA

7. Applications

- Broadcast Equipment
- Satellite Video/Audio Transmission Equipment
- Medical Imaging Devices
- IPTVs Distributing
- Video Surveillance Cameras
- Video Conferencing Devices
- Digital Cinemas
- Aerospace Application
- Military Application

8. MPEG-2 Video Decoder IP Core Integration Sheet

The decoder IP core is delivered as a ready-to-use netlist core for FPGAs. Figure-4 shows the inputs and outputs of the decoder core.

The MPEG-2 video decoder IP core integration details are provided in a separate Integration Sheet upon delivery of the IP core.

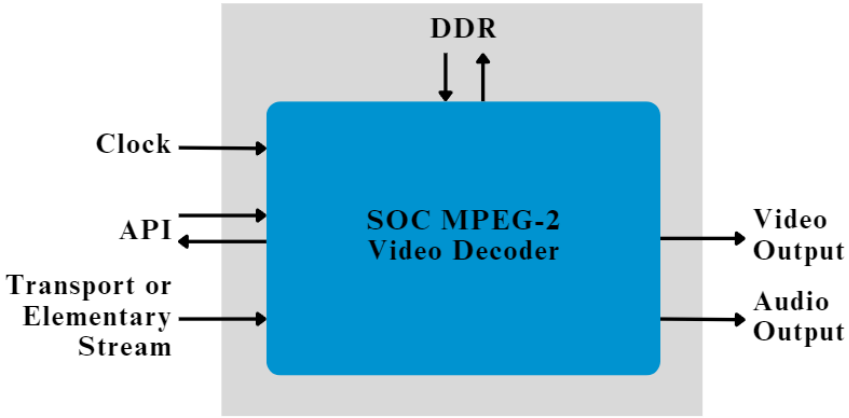

Figure-4 The inputs and outputs of the MPEG-2 video decoder IP core

9. The SOC Product Code Format

SOC integrates all products into one Product Code system as shown in Figure-5.

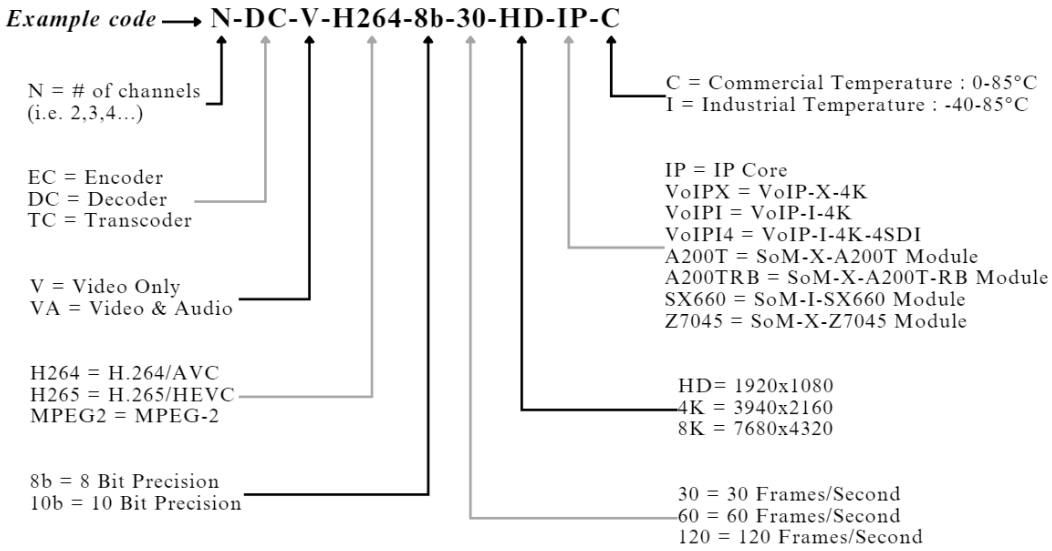

Figure-5 SOC Product Code Format Example

10. User API

The decoder IP core is controllable through a user API, which allows the user to control the operations of the decoder by setting the control registers during runtime. Figure-6 shows an example of API reads and demonstrates the importance of maintaining the API address for 4 clock cycles in order to process the read. Figure-7 shows an example of API writes and demonstrates the importance of waiting 3 clock cycles between writes to allow the system to process the write. Refer to the *MPEG-2 Decoder API* manual for specific registers and functions.[4]

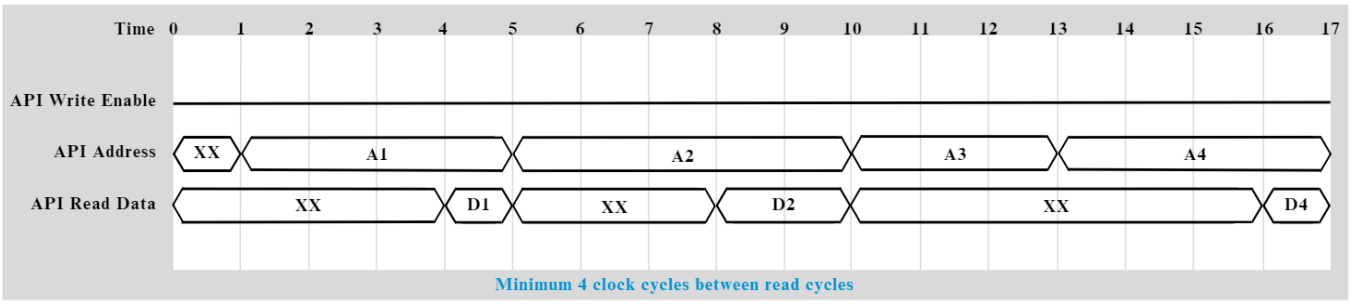

Figure-6 Example of an API read

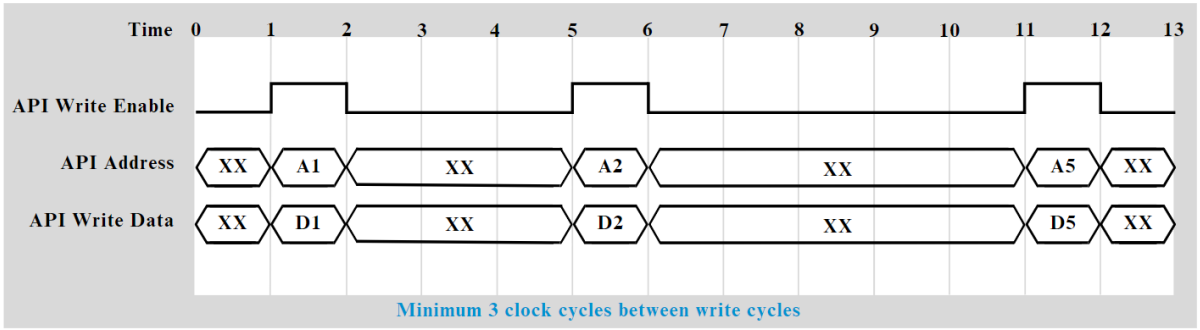

Figure-7 Example of an API write

[4] The API settings are reset to their generic values between power cycles.

11. Technical Support

SOC can provide technical support for all of its products, which includes documentation, IP core upgrading, e-mail, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

12. IP Core Upgrades

Upgrades to the IP core are available to all the delivery formats provided by SOC. Upgrades are part of the technical support contract signed individually. There are upgrade programs available for subscription after the technical support period ends.

13. Related Information

SOC offers encoders, decoders, and transcoders from various standards including H.265, H.264, and MPEG-2. Additionally, SOC provides solutions for video scaling, overlays, metadata, closed captioning, and more.

14. Ordering Information

The SOC MPEG-2 video/audio decoder IP cores are available for licensing, a one-time fee purchase, or a combination of one-time fee plus reduced royalty payments. Alternatively, modules can be ordered on a unit by unit basis with the IP core already integrated. Refer to the SoM Module Datasheets, such as the *SoM-X-A200T Module Datasheet*, for more information on the modules.

Please contact the SOC sales department by telephone at +1(519) 880-8609 or by email at : sales@soctechnologies.com

15. Document Revisions

Version #	Revision Date	Notes
V.6.0	2024/07/02	Initial Revision