

# **SOC H.264 Video Encoder IP Core Datasheet**

System-On-Chip (SOC) Technologies

Revision 7.0

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# 1. Product Overview

The SOC H.264/AVC (H.264) video encoder is a single core solution that supports single or multi-channel H.264 video encoding for all industry standard resolutions including QVGA, SD, HD, 4K up to 120fps, and 8K up to 60fps.

SOC can provide the H.264 video encoder IP core for AMD (Xilinx) and Intel (Altera) FPGAs. SOC also offers an all-in-one encoder module based on the H.264 video encoder IP core.

The SOC H.264 video encoder is implemented based on SOC’s proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has the significant advantages of high-speed (low latency) and small footprint (low power), while still providing high video quality and high resolution.

The SOC H.264 IP core is a High Profile encoder with Baseline and Main Profiles available, providing a subset of features in order to fit smaller FPGAs. It encodes either 4:2:0 or 4:2:2 streams, and has both 8-bit and 10-bit depth support. The 8-bit encoder is best suited for consumer products, while the 10-bit is for high-end applications such as broadcasting, digital cinema, military, aerospace, and medical devices.

Users are able to control the operations of the encoder using the integrated user API which allows for customization of the encoder settings such as Constant Bit Rate (CBR), Variable Bit Rate (VBR), bit depth, HDR, etc. The API user manual is provided with the IP core and module.

The H.264 encoder core can be customised into the following versions:

- 1. Standard Version:**  
A balanced system optimised for key factors of logic resource utilisation and performance supporting I+P GOP structure.
- 2. I-Frame Version:**  
The I-Frame version implements intra-prediction (I-Frames) only, without motion vector predictions. This reduces the logic resources and simplifies encoder complexity, allowing for very high channel density in a single FPGA.

Key Features	
Profile & Level	High Profile (up to 6.1L)
Chroma Format	4:2:0 or 4:2:2
Resolution	SD, HD, 4K, 8K and custom
Frame Rate	Up to 120fps
Precision	8 or 10 bits
Input Stream	Transport or Elementary
Latency	0.25 - 4 frames

**3. Slim Version:**

The slim version is optimised for low logic resources which uses significantly less resources compared to the standard version. This reduction of resources results in lower picture quality. Only 8bit encoding is supported.

**4. B-Picture Version:**

Using bi-predicted B pictures, a high compression efficiency is achieved. This version requires the most logic resources and has a higher encoding latency.

**5. Other Versions:**

Other special versions of the SOC H.264 encoder, such as multi-channel and video scaling, are also available. Please contact SOC for product details.

The SOC encoder series can be integrated with an audio encoder to provide an all-in-one encoding solution. SOC can also integrate network modules, UDP-IP, Ethernet MACs, as well as a MPEG transport stream multiplexer into the design to produce full system-on-chip systems.

## 2. The SOC H.264/AVC Video Encoder Architecture

The SOC H.264 video encoder is a self-contained FPGA IP core that can be either placed as a standalone core into a single FPGA or integrated with other logic blocks in the same FPGA for custom applications.

The block diagram of the IP core can be seen in Figure-1. All of the blocks in the design are implemented in hardware without embedded processors or embedded software, which offers high speed, low logic resource consumption, and low power.

Input to the encoder is a standard video pixel stream in 4:2:2 format. The output of the encoder is a transport stream which includes the video and any audio or metadata. Alternatively, the encoder can output the video as an elementary stream.

The SOC H.264 encoder requires one external clock source. The video uses an independent clock which can be in the range of 13.5-148.5 MHz. The encoder also requires an external DDR3 or DDR4 memory with a minimum size depending on the highest resolution the user wishes to achieve as well as the core's requirements. See section 6 "Targeted FPGAs and Logic Resources" for more information.

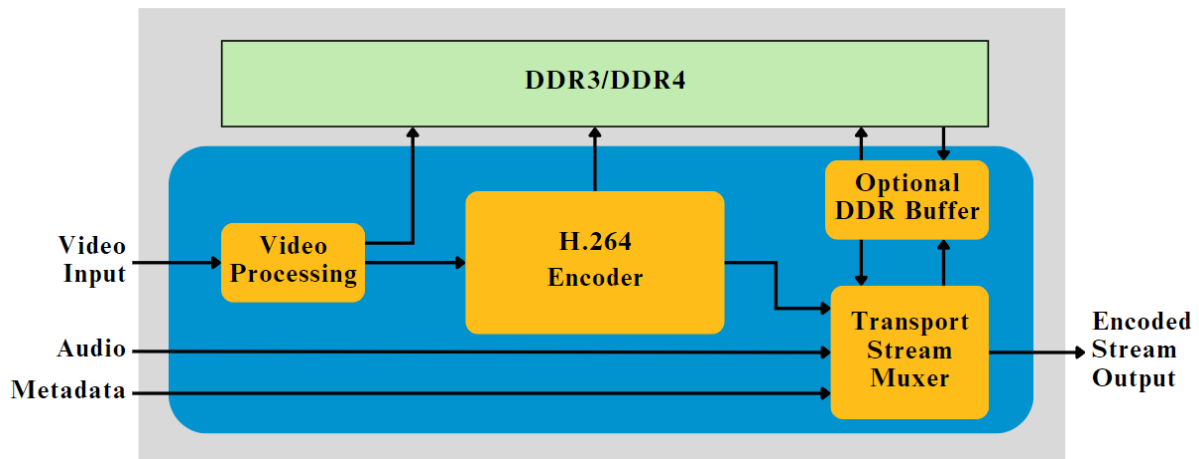


Figure-1 Block Diagram of SOC H.264 Video Encoder

### 3. The H.264 and Audio Encoder Solutions

SOC provides three H.264 and audio encoder solutions:

#### 1. **FPGA-DSP Solution:**

For FPGAs that do not have an embedded ARM processor, an external DSP is used for audio encoding. Figure-2 shows the architecture of this system. The audio signal is sent to the external DSP (Blackfin BF512) for encoding. The encoded audio stream is sent back to the FPGA, which is muxed into the transport stream by the transport encoder in the FPGA.

#### 2. **Single FPGA Solution:**

For FPGAs that have an embedded ARM processor, the ARM processor is used for audio encoding while the video encoder IP core uses the logic part of the FPGA. Figure-3 provides a block diagram for this single chip solution. The user must instantiate the HPS/PS for the system to work correctly. A guide for this will be provided with delivery of the IP core or module.

#### 3. **PCM Pass Through Solution:**

Audio data can be inserted into the transport stream as raw PCM data.

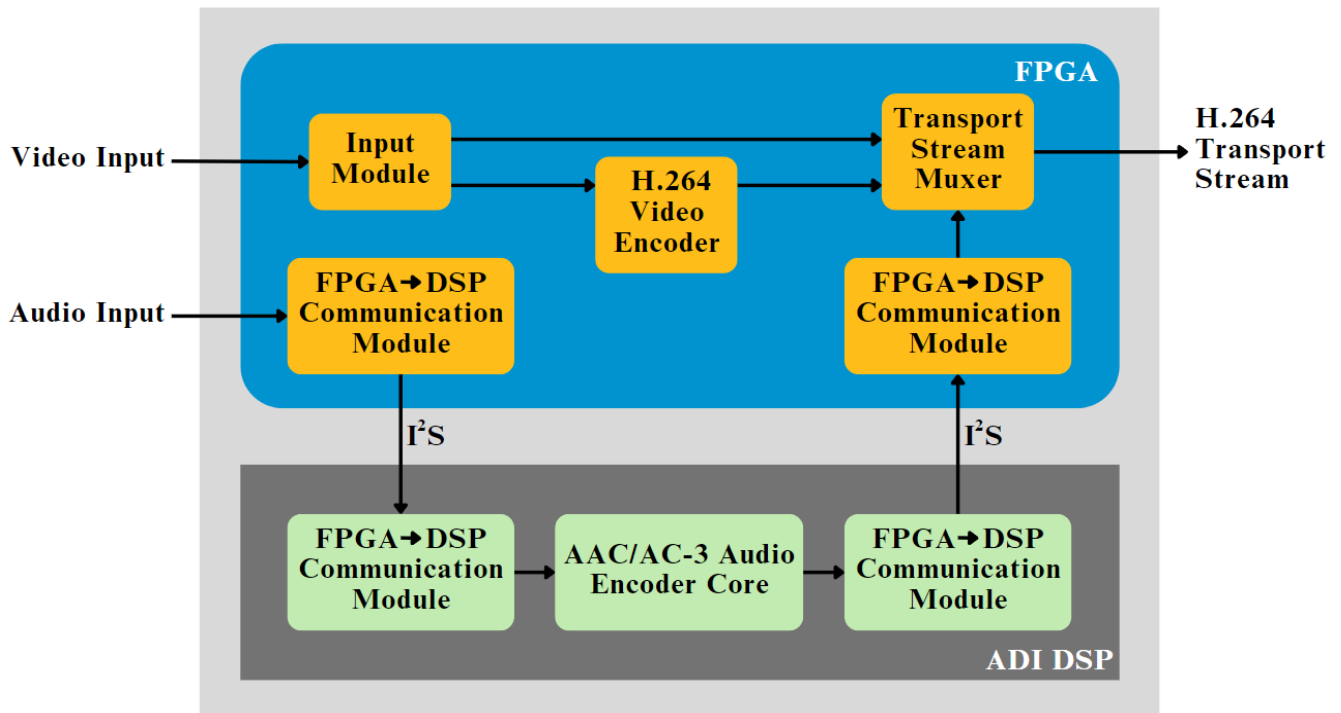


Figure-2 Block Diagram of the FPGA-DSP Video/Audio Encoder Solution

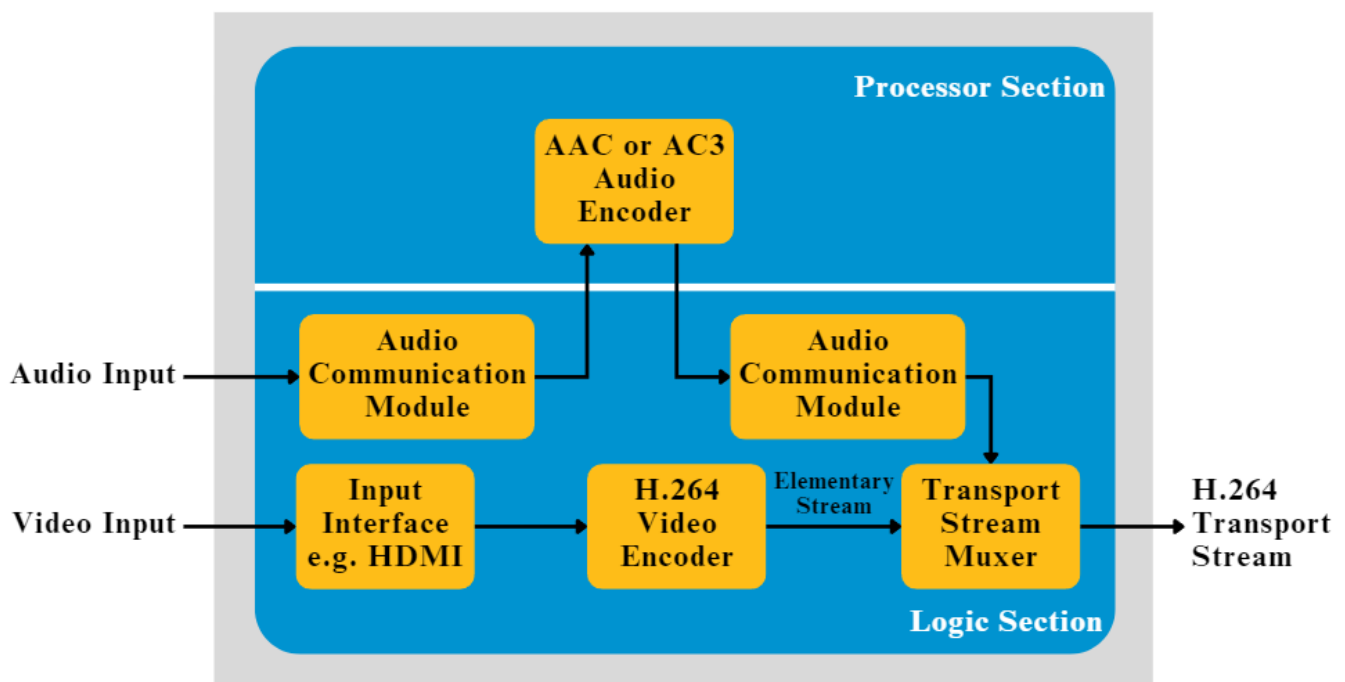


Figure-3 Block Diagram of the Single FPGA Video/Audio Encoder Solution

## 4. Video Technical Specifications

**Conformance Standard:**

H.264/AVC (ISO/IEC 14496-10)

**Profiles:**

- High Profile
- Main Profile
- Baseline Profile

**Chroma Format:**

- 4:2:0
- 4:2:2

**Precision:**

- 8 bits
- 10 bits

**Resolution:**

- 640x480 (QVGA)
- 1280x720 (SD)
- 1920x1080 (HD)
- 3940x2160 (4K)
- 7680x4320 (8K)
- Other resolutions available upon request

**Frame Rate:**

The SOC encoder supports all industry standard frame rates, including the following:

- 10fps
- 29.97fps
- 30fps
- 50fps
- 59.95fps
- 60fps
- 120fps
- Other frame rates available upon request

**Supported Frame Types:**

- I Frame
- P Frame
- B Frame

**Latency:**

The SOC H.264 encoder has very low latency due to its hardware implementation. Table-1 shows the different encoding engine latencies depending on performance requirements.

Latency	Supported GOP	Performance
< ¼ Frame	I, I+P	Standard
1 Frame	I, I+P	High
2-4 Frames	I, I+P, I+P+B	Very High

Table-1 The latency associated with each supported GOP and its associated performance

**Bit Rate:**

- Constant Bit Rate (CBR) - User controllable through API
- Variable Bit Rate (VBR) - User controllable through API

**Power:**

The power consumption that the IP core uses is based on many factors such as resolution, frame rate, number of channels, and core settings. Table-2 shows the power consumption for the different versions at a resolution of 1920x1080 and frame rate of 60 fps.<sup>1</sup>

Version	Power Consumption
Standard	2.6W
I-Frame	1.7W
Slim	1.9W
B-Picture	3.3W

Table-2 The power consumption associated with each version at 1920x1080 @60fps

<sup>1</sup> Power consumption estimates are for the encoder core only and do not include the vendor DDR controller or external memory.



## 5. Audio Technical Specifications

**Conformance Standard:**

HE-AAC (ISO/IEC 14496-3), MPEG-2 Layer-2

**Audio Sample Rate:**

- 44.1 kHz
- 48 kHz

**Audio Bit Rate:**

The total audio bit rate for stereo (left and right) audio encoding mode. Table-3 describes the different audio bit rates associated with each audio solution.

Audio Solution	Bit Rate (kbps)
FPGA-DSP	32-128
FPGA-ARM	16-384

Table-3 Audio bit rate for each audio solution

## 6. Target FPGAs and Logic Resources

The SOC H.264 encoder IP core is available for both Xilinx and Altera FPGAs as long as they meet the logic resource and clock speed requirements.

Logic resources are for the **CODEC only**. Additional resources are required depending on the final IP core design requirements (Transport Stream Support, Resolution requirement, Input video mode, DDR Configuration etc..).

### DDR3/DDR4 Memory Minimum Based on Resolution

The encoder core requires a certain amount of DDR memory capacity and bandwidth in order to run. The requirements change depending on the highest resolution and core features the user desires. SOC's encoder core supports the use of a BRAM cache to reduce DDR bandwidth. Table-4 describes the DDR requirements based on 1 channel 60fps and 8 bit pixel depth.<sup>2</sup>

Resolution	DDR Memory Capacity	Bandwidth (Gbps)				
		I Frame Only <sup>3</sup>	With Cache		No Cache	
			I+P	I+P+B	I+P	I+P+B
HD or lower	128 Mbytes	4.4	9.9	13.2	13.2	25.8
4K	512 Mbytes	17.6	39.6	52.8	52.8	103.2
8K	2 Gbytes	70.4	158.4	211.2	211.2	412.8

Table-4 The DDR3/DDR4 memory requirements

<sup>2</sup> 10 bit requires 30% more bandwidth and double the capacity

<sup>3</sup> I Frame Only can be accomplished without DDR if enough BRAM resources are available

### Logic Resources on Xilinx FPGAs

The logic resources required on Xilinx FPGAs by the encoder IP core are listed in the following table. URAM can be used on available devices. Table-5 describes the resource usage for HD streams.

Resource Type	Version				
	Standard-	I-Frame	Slim	B-Frame	Cache Feature
LUTs	98K	68K	75K	125K	1K
B-RAM	9.1Mb	4.6Mb	5.7Mb	10.8Mb	2.6Mb (Min) 5.2Mb (Std)
DSPs	172	35	97	196	0

Table-5 Logic resource utilisation of the HD encoder on a Xilinx FPGA

### Logic Resources on Altera FPGAs

The logic resources required on Altera FPGAs by the encoder IP core are listed in the following table. Table-6 describes the resource usage for HD streams.

Resource Type	Version				
	Standard	I-Frame	Slim	B-Frame	Cache Feature
ALMs	61K	43K	47K	78K	1.6K
B-RAM	9.1Mb	4.6Mb	5.7Mb	10.8Mb	2.6Mb (Min) 5.2Mb (Std)
DSPs	172	35	97	196	0

Table-6 Logic resource utilisation of the HD encoder on an Altera FPGA

## 7. Applications

- Broadcast Equipment
- Satellite Video/Audio Transmission Equipment
- Medical Imaging Devices
- IPTVs Distributing
- Video Surveillance Cameras
- Video Conferencing Devices
- Digital Cinemas
- Aerospace Application
- Military Application

## 8. H.264 Video Encoder IP Core Integration Sheet

The encoder IP core is delivered as a ready-to-use netlist core for FPGAs. Figure-4 shows the inputs and outputs of the encoder core.

The H.264 video encoder IP core integration details are provided in a separate Integration Sheet upon delivery of the IP core.

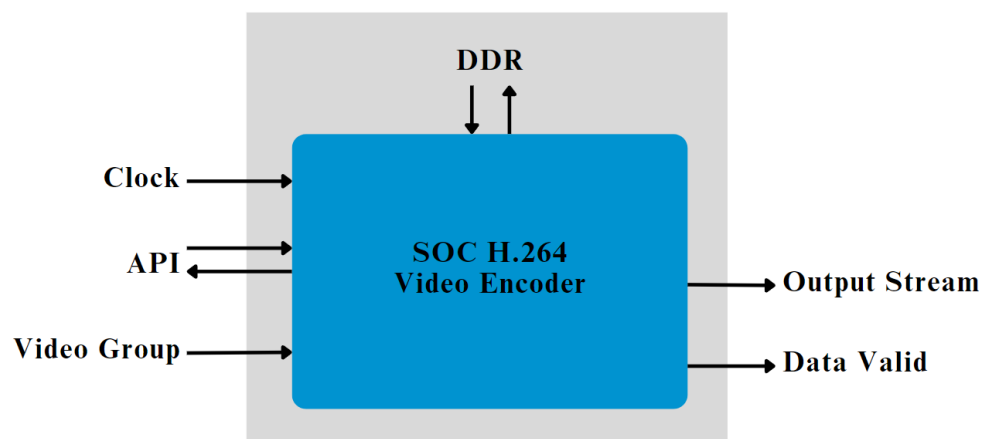


Figure-4 The inputs and outputs of the H.264 video encoder IP core

# 9. The SOC Product Code Format

SOC integrates all products into one Product Code system as shown in Figure-5.

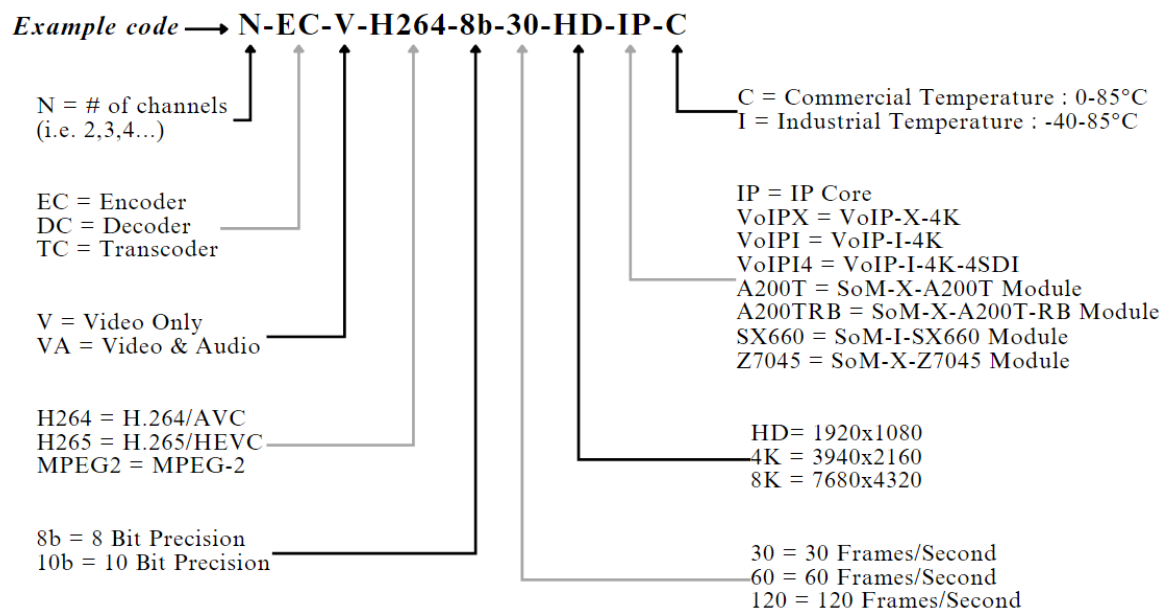


Figure-5 SOC Product Code Format Example

# 10. User API

The encoder IP core is controllable through a user API, which allows the user to control the operations of the encoder by setting the control registers during runtime. Figure-6 shows an example of API reads and demonstrates the importance of maintaining the API address for 4 clock cycles in order to process the read. Figure-7 shows an example of API writes and demonstrates the importance of waiting 3 clock cycles between writes to allow the system to process the write. Refer to the *H.264 Encoder API* manual for specific registers and functions<sup>4</sup>.

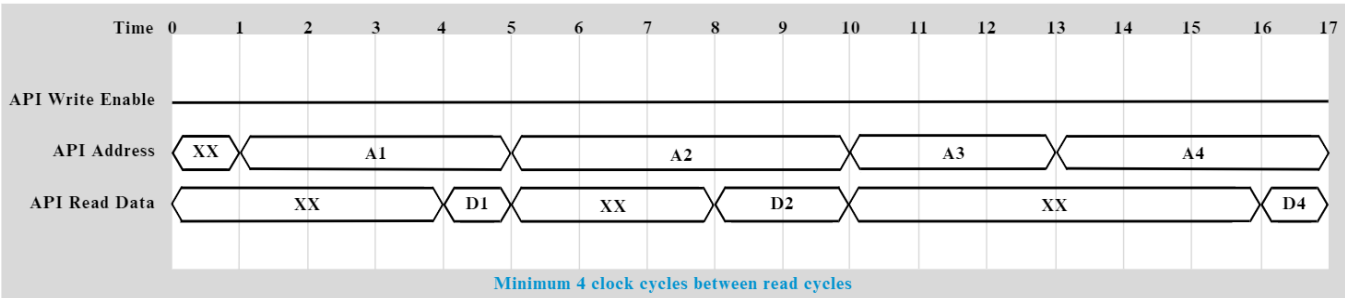


Figure-6 Example of an API read

<sup>4</sup> The API settings are reset to their generic values between power cycles.

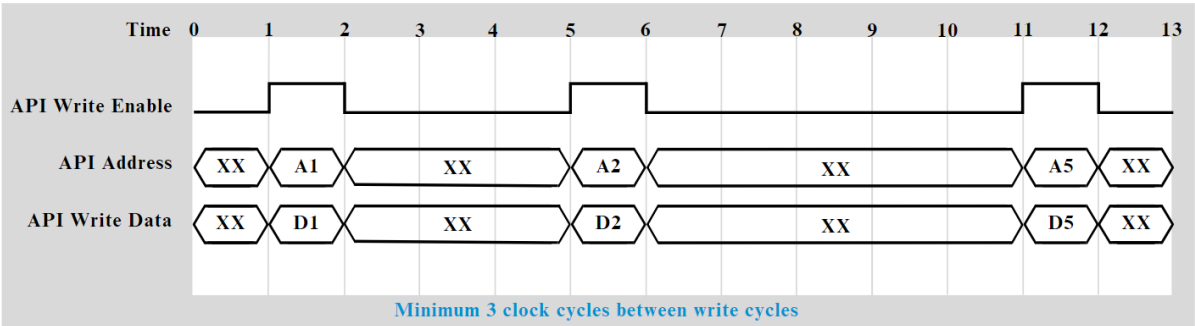


Figure-7 Example of an API write

## 11. Technical Support

SOC can provide technical support for all of its products, which includes documentation, IP core upgrading, e-mail, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

## 12. IP Core Upgrades

Upgrades to the IP core are available to all the delivery formats provided by SOC. Upgrades are part of the technical support contract signed individually. There are upgrade programs available for subscription after the technical support period ends.

## 13. Related Information

SOC offers encoders, decoders, and transcoders from various standards including H.265, H.264, and MPEG-2. Additionally, SOC provides solutions for video scaling, overlays, metadata, closed captioning, and more.

## 14. Ordering Information

The SOC H.264 video/audio encoder IP cores are available for licensing, a one-time fee purchase, or a combination of one-time fee plus reduced royalty payments. Alternatively, modules can be ordered on a unit by unit basis with the IP core already integrated. Refer to the SoM Module Datasheets, such as the *SoM-X-A200T Module Datasheet*, for more information on the modules.

Please contact the SOC sales department by telephone at +1(519) 880-8609 or by email at : [sales@soctechnologies.com](mailto:sales@soctechnologies.com)

# 15. Document Revisions

Version #	Revision Date	Notes
V.7.0	2024/06/27	Full Datasheet Update – Initial release